

Features

- Low power consumption
- Low temperature coefficient
- Built-in hysteresis characteristic
- High input voltage (up to 8V)
- Output voltage accuracy:
 $\pm 2\% @ V_{DET} \geq 2.5mV$
 $\pm 50mV @ V_{DET} < 2.5mV$
- SOT23-3 and SOT23 package

Applications

- Battery checkers
- Level selectors
- Power failure detectors
- Microcomputer reset
- Battery memory backup
- Non-volatile RAM signal storage protectors

General Description

The CXM61C series devices are a set of three terminal low power voltage detectors implemented in CMOS technology. Each voltage detector in the series detects a particular fixed voltage ranging from 0.9V to 5.0V. The voltage detectors consist of a high-precision and low power consumption standard voltage source as well as a comparator,

hysteresis circuit, and an output driver (CMOS inverter or NMOS open drain). CMOS technology ensures low power consumption.

Although designed primarily as fixed voltage detectors, these devices can be used with external components to detect user specified threshold voltages.

Selection Table	Det. Voltage	Hys. Width	Output	Tolerance	Package
CXM61CC0902MR	0.9V	4%	CMOS	$\pm 50mV$	SOT23-3 SOT23
CXM61CN0902MR	0.9V	4%	NMOS	$\pm 50mV$	
CXM61CC1002MR	1.0V	4%	CMOS	$\pm 50mV$	
CXM61CN1002MR	1.0V	4%	NMOS	$\pm 50mV$	
...	
CXM61CC2402MR	2.4V	4%	CMOS	$\pm 50mV$	
CXM61CN2402MR	2.4V	4%	NMOS	$\pm 50mV$	
CXM61CC2502MR	2.5V	4%	CMOS	$\pm 2\%$	
CXM61CN2502MR	2.5V	4%	NMOS	$\pm 2\%$	
...	$\pm 2\%$	
CXM61CC5002MR	5.0V	4%	CMOS	$\pm 2\%$	
CXM61CN5002MR	5.0V	4%	NMOS	$\pm 2\%$	

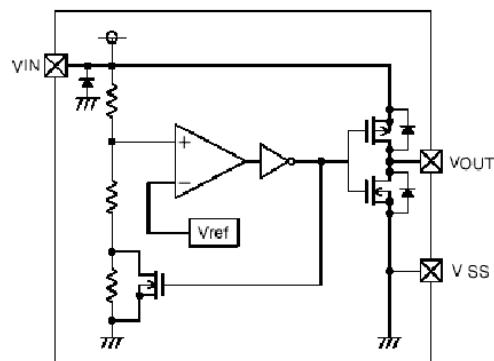
Order Information

CXM61C①②③④⑤⑥⑦

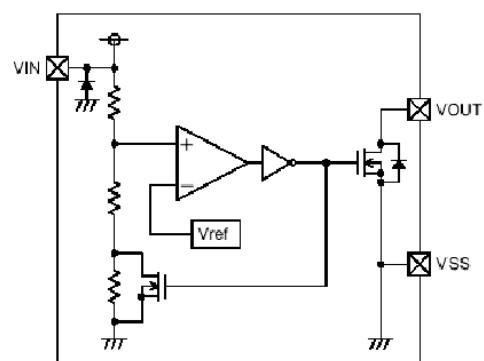
Designator	Symbol	Description
①	C N	CMOS output NMOS output
②③	VOUT	Output Voltage(0.9~5.0V)
④⑤	O2	Standard
⑥	M N	Package:SOT23-3 Package:SOT23
⑦	R G	RoHS / Pb Free Halogen Free

Block Diagram

(1) CMOS Output

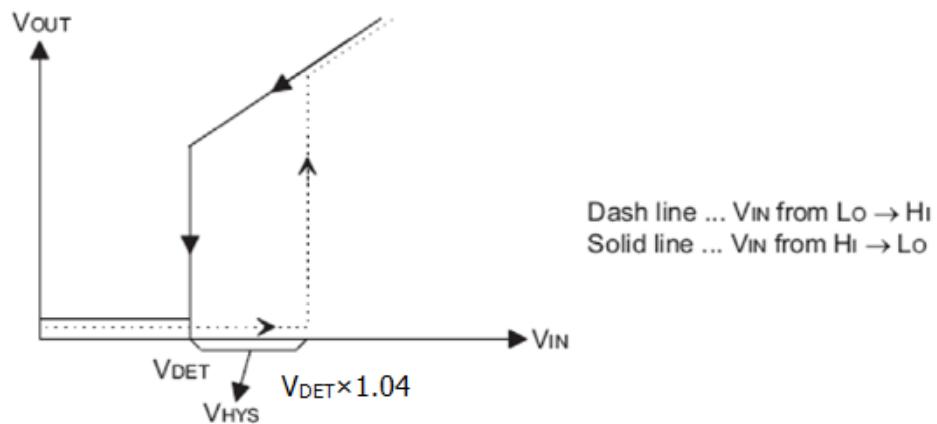


(2) N-ch Open Drain Output

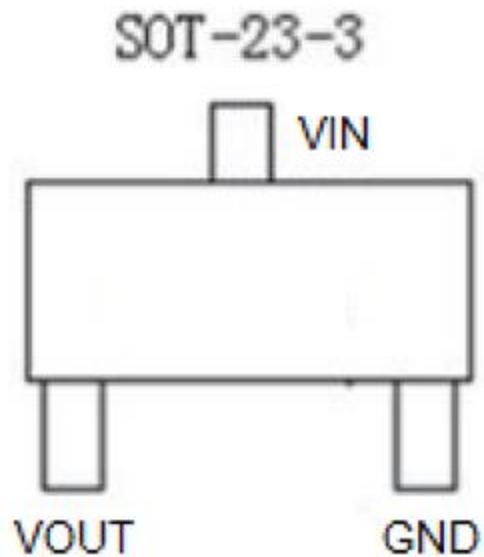


Output Table & Curve

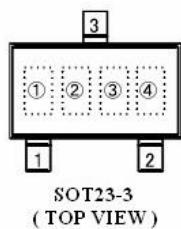
V_{DD}	$V_{DD} > V_{DET}(+)$	$V_{DD} \leq V_{DET}(-)$
V_{OUT}	Hi-Z	V_{SS}



Pin Assignment



Marking Rule



① Represents integer of detect voltage and CMOS Output

MARK	CONFIGURATION	VOLTAGE (V)
A	CMOS	0.X
B	CMOS	1.X
C	CMOS	2.X
D	CMOS	3.X
E	CMOS	4.X
F	CMOS	5.X
H	CMOS	6.X

N-Channel Open Drain Output

MARK	CONFIGURATION	VOLTAGE (V)
K	N-ch	0.X
L	N-ch	1.X
M	N-ch	2.X
N	N-ch	3.X
P	N-ch	4.X
R	N-ch	5.X
S	N-ch	6.X

② Represents decimal number of detect voltage

MARK	VOLTAGE (V)	MARK	VOLTAGE (V)
0	X.0	5	X.5
1	X.1	6	X.6
2	X.2	7	X.7
3	X.3	8	X.8
4	X.4	9	X.9

③ Represents accuracy

MARK	ACCURACY
3	2%
1	1%

④ Represents production lot number

Based on the internal standard. (G, I, J, O, Q, W excepted)

Absolute Maximum Ratings

Supply Voltage-0.3V to 8V Storage Temperature-50°C to 125°C
 Operating Temperature-40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Thermal Information

Symbol	Parameter	Package	Max.	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient) (Assume no ambient airflow, no heat sink)	SOT23-3	500	°C/W
P_D	Power Dissipation	SOT23-3	0.20	W

Note: P_D is measured at $T_a = 25^\circ\text{C}$

Electrical Characteristics

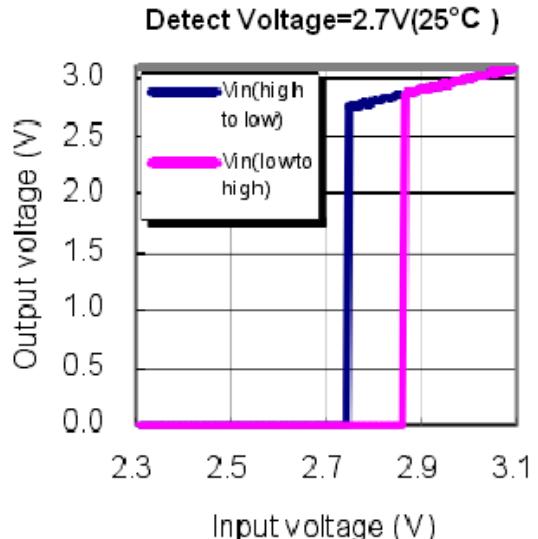
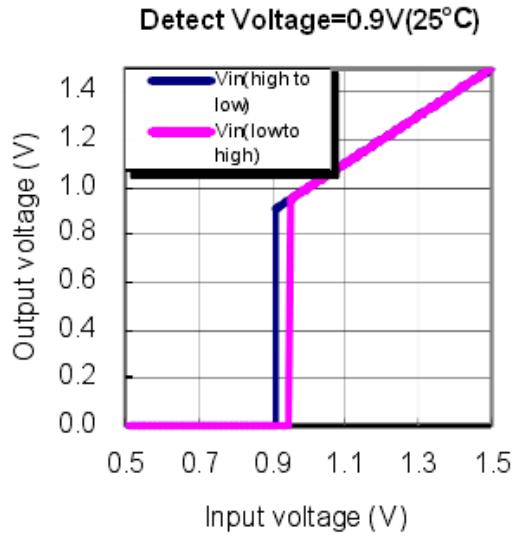
$V_{DF}=0.8\text{V}\sim 5.0\text{V}$

$T_a=25^\circ\text{C}$

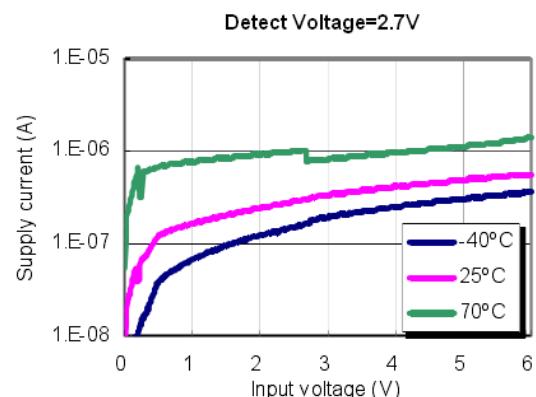
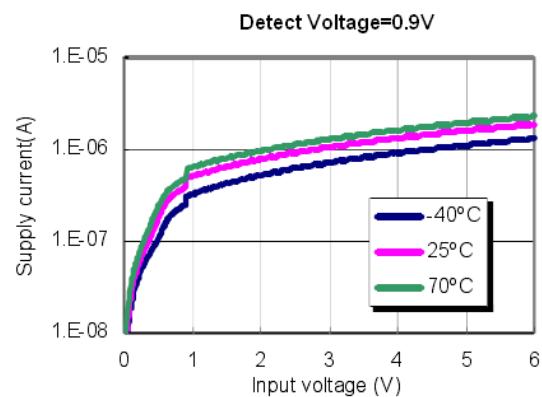
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DET}	Detection Voltage	$V_{DF}=0.9\text{V}\sim 2.4\text{V}$		$V_{DET}-0.05$	V_{DET}	$V_{DET}+0.05$	V
		$V_{DF}=2.5\text{V}\sim 5.0\text{V}$		$V_{DET}*0.98$	V_{DET}	$V_{DET}*1.02$	V
V_{HYS}	Hysteresis Width	-		$0.02*V_{DET}$	$0.05*V_{DET}$	$0.10*V_{DET}$	V
I_{DD}	Operating Current	$V_{in}=1.5\text{V}$		-	0.7	2.3	μA
		$V_{in}=2.0\text{V}$		-	0.8	2.7	
		$V_{in}=3.0\text{V}$		-	0.9	3.0	
		$V_{in}=4.0\text{V}$		-	1.0	3.2	
		$V_{in}=5.0\text{V}$		-	1.1	3.6	
V_{DD}	Operating Voltage	-	-	0.7	-	10	V
I_{OL}	Output Sink Current	2V	$V_{OUT}=0.2\text{V}$	0.5	1	-	mA
$\frac{\Delta V_{DET}}{V_{DF}\Delta T_a}$	Temperature Coefficient	-	-25°C $<Ta<125^\circ\text{C}$	-	± 100	-	ppm/°C

Typical Performance Characteristics

(1) Output Voltage vs Input voltage



(2) Supply Current vs. Input Voltage

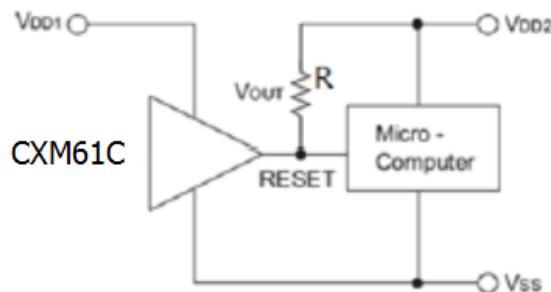


Application Circuits

Microcomputer Reset Circuit

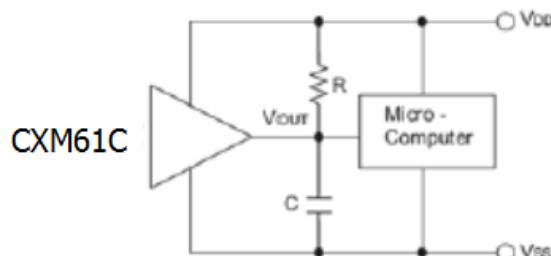
Normally a reset circuit is required to protect the microcomputer system from malfunctions due to power line interruptions. The following examples show how different output configurations perform a reset function in various systems.

NMOS open drain output application for separate power supply



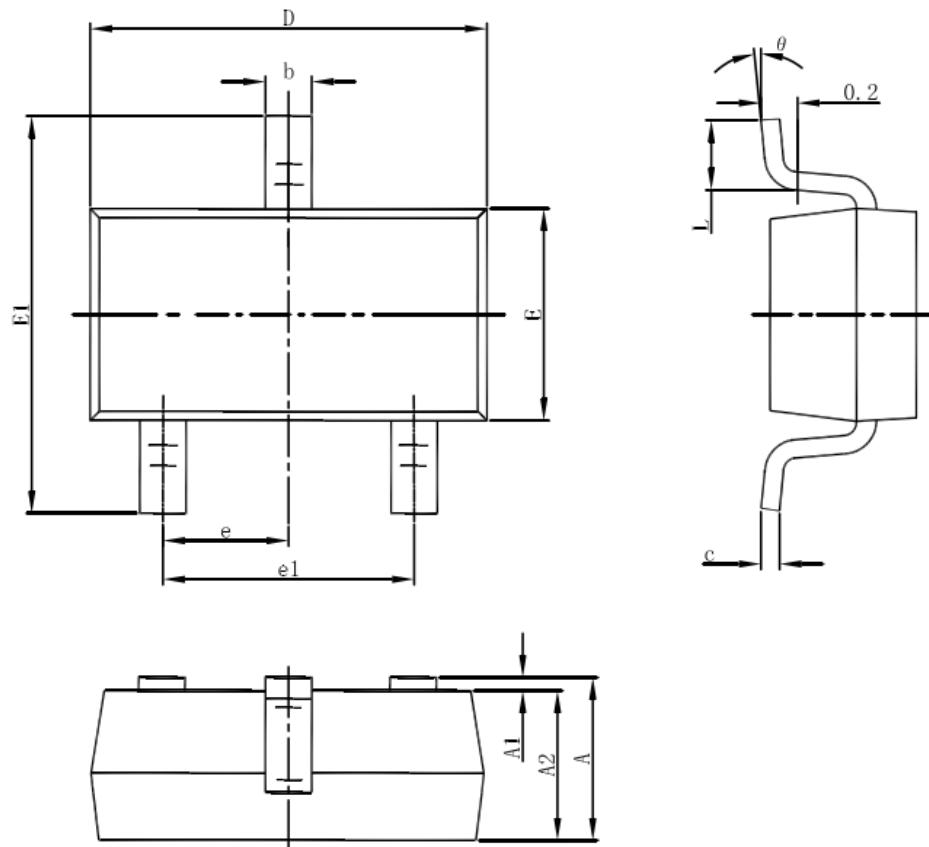
R=47K

NMOS open drain output application with R-C delay

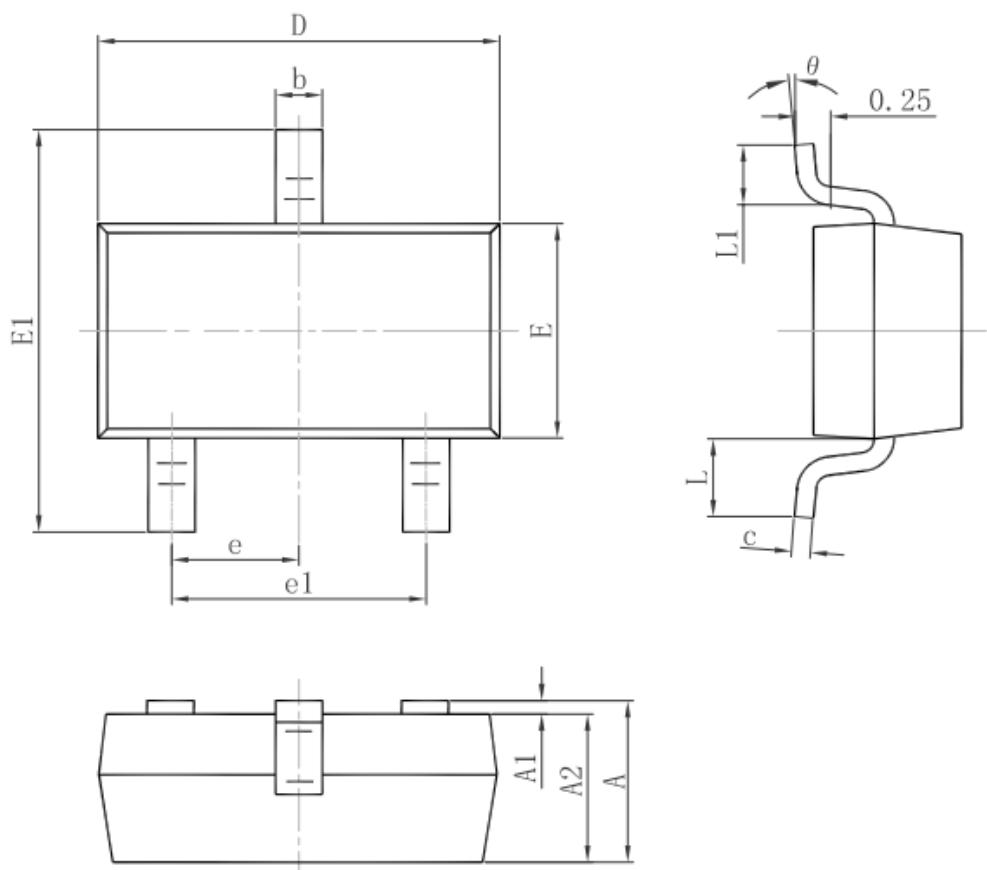


Package Information

3-pin SOT23-3 Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

3-pin SOT23 Outline Dimensions


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°



CXM61CN series

Copyright © by CXMCHIP SEMICONDUCTOR Co.,Ltd.

CXMCHIP SEMICONDUCTOR Co.,Ltd. 保留权利在任何时候变更或终止产品，对于说明书的使用不负任何责任，建议客户在使用或下单前与我们取得最新、最正确的产品信息。

文中提到的应用目的仅仅是用来说明，*CXMCHIP SEMICONDUCTOR Co.,Ltd.* 不保证或表示这些没有进一步修改的应用将是适当的，也不推荐本产品使用在会由于故障或其它原因可能会对人身造成危害的应用，不授权使用于救生、维生器件或系统中作为关键器件。*CXMCHIP SEMICONDUCTOR Co.,Ltd.* 有不事先通知而修改产品的权利。